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A Modified Series Z-Source Inverter Based on Switched Inductors with a High Voltage Gain and a Reduced Voltage Stress on Capacitors

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Abstract
In this paper, a series Z-source inverter based on a switched inductor cell is proposed for the first time. This inverter is able not only to increase the voltage gain, in comparison with the conventional Z–source inverters, but also to solve the ST (shoot-through) state's problems. In this inverter, the value of the voltage gain is increased by an increase in the number of used diodes and inductors in the switched inductor cells. The low value of the capacitors' voltage stress is another advantage of the proposed inverter. The voltage of the capacitors is increased from zero to the desired value by increasing the duty cycle of ST state from zero to the desired value. This leads to a soft start in the proposed inverter, which is impossible in conventional Z-source inverters. In this paper, in addition to investigating the operation of the proposed inverter in different operating modes, the value of voltage stress of the capacitors, current inductors, and the value of voltage gain are also calculated. Moreover, the proposed inverter is compared with the conventional Z-source inverters to investigate the advantages and disadvantages of it. Finally, the accuracy performance of the proposed inverter is verified through the simulation results in PSCAD/EMTDC software programs.

Keywords: Full-Bridge Inverter, Shoot-Through, Switched Inductors, Voltage Gain, Z-source.

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1. Introduction

Current source inverters and voltage source inverters are two main kinds of conventional inverters. In the voltage source inverter, the effective value of output voltage is lower than the magnitude of input voltage; therefore, this kind of inverter is known as step-down voltage. In current source inverters, the effective value of output voltage is higher than the magnitude of input voltage. Therefore, this kind of inverter is known as step-up voltage. In high and low voltage applications, a dc-dc converter with the capability of increasing and / or decreasing voltage is used before dc voltage link. This leads to an increase in the complexity and the cost of the inverter.

In order to overcome these problems, full-bridge and half-bridge Z-source inverters have been presented in [1, 2]. These inverters are able to increase and decrease voltage and consist of two inductors and two capacitors in an X shape impedance network which connects the bridge of the inverter to dc voltage sources. The dc link voltage is increased by a short circuit on inverter's legs. As a result, the effective value of load ac voltage is increased. It is important to note that when the input voltage is high enough it is avoided from ST state, and in this condition, this inverter acts the same as a buck voltage source inverter. The control methods of this inverter have been investigated in [3-5]. In addition, modeling, the design of the controller [6-8] and its fields of applications [9-11] have been investigated in literature.

In a conventional Z-source inverter, the voltage stress of capacitors is very high, and there is discontinuity in the source current; therefore, in order to overcome this problem, a new Z-source inverter, called embedded Z-source inverter (EZSI), has been presented [12]. In this inverter, there is not a common earth between the inverter and an input voltage source. In addition, there are two sources in symmetric EZSI. These are two main disadvantages of this inverter. In [13], in order to decrease the nominal value of the passive elements in conventional Z-source inverters and to maintain the continuity of the source current, a quasi Z-source inverter (QZSI) has been presented. In [14-15], two developed topologies of this inverter that are called a diode-assisted quasi Z-source Inverter (DQZSI), and a capacitor-assisted quasi Z-source inverter (CQZSI), with the aim of increasing the voltage gain, have been presented. In order to overcome the high value of the inrush current, a series Z-source inverter has been presented [16]. In this inverter, the impedance network consists of a series connected to the input dc voltage sources, which leads to having the same earth between the inverter and the dc voltage source. In addition, the value of the voltage stress of capacitors is lower than other conventional Z-source inverters. The control method of this inverter, the suitable design of its elements, and the method of using photovoltaic systems connected to the grid to maximize their power point tracking have been presented in [17-19]. One of the main problems of the series Z-source inverters is the voltage gain that is the same as conventional Z-source inverters. In order to increase the voltage gain, the series' array of Z-source inverter has been presented [20-21]. One of the main problems of this topology is the high number of used dc voltage sources and capacitors. Therefore, the other topology which is called L-Z-source inverter has been presented in [22]. This inverter includes different advantages such as a non-high inrush current; however, it is necessary to use high value of duty cycle in ST state to generate high voltage gain. In [23], an improved topology for impedance source inverter, based on the presented cell in [22] and a transformer, has been presented. Due to the use of a transformer, the design of this inverter is difficult and has all problems of the transformer-based structures.

In this paper, a series full-bridge Z-source inverter with a high voltage gain is proposed. The high voltage gain in this topology, in comparison with the conventional Z-source inverters, is obtained because of using a switched inductor cell. The same earth between the inverter and the voltage source and its low voltage stress of capacitors are two other advantages of this inverter in comparison with other Z-source inverters. The topology, the operation, and the steady state analysis of the proposed inverter in different operating modes are presented. Then, the voltage stress of capacitors, the inductor's current, and the voltage gain of the developed proposed

inverter, based on a switched inductor's cell that includes n numbers of inductors are calculated. In addition, the proposed inverter is compared with the conventional Z-source inverters. At the end, the correct performance of the proposed inverter is reconfirmed by simulation results on EMTDC/PSCAD software programs.

2. Proposed Inverter Topology

The proposed Z-source inverter topology is shown in Fig. 1. As shown in this figure, the proposed inverter consists of two switched inductor cells in its structure. The first cell consists of inductors $L_{1,1}$, $L_{2,1}$ and diodes of $D_{1,1}$, $D_{2,1}$ and $D_{3,1}$ while the second cell includes inductors $L_{1,2}$, $L_{2,2}$ and diodes of $D_{1,2}$, $D_{2,2}$ and $D_{3,2}$. The input voltage source of V_i, diode D, the capacitors of C_1, C_2 and the power switches of S_1, S_2, S_3, and S_4 from its inverter section are the other used devices in the proposed Z-source topology.

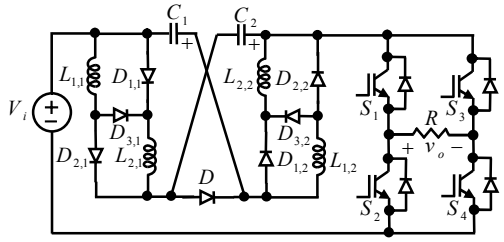


Fig. 1: The proposed topology

In order to simplify the analysis of the proposed inverter, it is assumed that:

- All used elements are ideal.
- The dead time for excitation pulses is ignored.
- It is assumed that $L_{1,1}=L_{2,1}=L_{1,2}=L_{2,2}=L$ and $C_{1,1}=C_{2,1}=C_{1,2}=C_{2,2}=C$.
- The values of all capacitances are considered very high.
- The resistance load is considered.

In the next section, the proposed inverter is completely analyzed in its three operating modes.

2.1. Operating Modes of the Proposed Inverter

The operating modes of the proposed inverter are determined based on the time interval that the inverter's switches are turned on or off, the state of the existed diodes in the first and second cells, and the diode D from turning on and off points of view. It is also resulted that the voltage of the capacitors C_1 and C_2 are equal in different operating modes because of the parallelism in the proposed Z-source inverter. Therefore, the current of these capacitors are also equal because the capacitance of both is the same.

2.1.1. First Operating Mode (Time Interval of $0 \le t < 0.5D_{ST}T_s$)

According to Fig. 2a, in the first time interval, all of the inverter's power switches are turned on, and the inverter is in short circuit state. Therefore, the inverter operates in ST state, and the voltage of the capacitors is decreased; this leads to a reduction in their stored energy. In addition, in such operating mode, the current of all inductors is increased, which causes an increase in their stored energy because their voltages are positive. Based on Fig. 2a it is resulted that:

$$v_{L1,1}=v_{L2,1} \quad (1)$$

$$v_{L1,2}=v_{L2,2} \quad (2)$$

According to the parallelism of the proposed inverter and based on (1) and (2), it is concluded that:

$$v_{L1,1}=v_{L2,1}=v_{L1,2}=v_{L2,2}=v_L \quad (3)$$

By applying KVL in Fig. 2a, we have:

$$-V_i+v_L-V_C=0 \quad (4)$$

As the switches of the inverter are turned on in this operating mode and the voltage of dc link is equal to zero, it is concluded that the output voltage is equal to:

$$v_o=0 \quad (5)$$

In this mode, based on Fig. 2a, the diode of D is turned off and by applying KVL in this figure and based on (4), its voltage-- which is a negative value-- is calculated as follows:

$$v_D=-2V_C-V_i \quad (6)$$

In addition, the voltage values of diodes of $D_{3,1}$ and $D_{3,2}$ that are negative values are obtained as follows:

$$v_{D3,1}=v_{D3,2}=-V_C-V_i \quad (7)$$

This operating mode is the same as the time interval of $0.5T_s \le t < 0.5(1+D_{ST})T_s$.

2.1.2. Second Operating Mode (Time Interval of $0.5D_{ST}T_s \le t < 0.5T_s$)

In the second operating mode, as shown in Fig. 2b, the switches of S_1 and S_4 are turned on and the switches of S_2 and S_3 are turned off. This leads to a positive voltage level at the output. In this operating mode, the voltage of capacitors is increased, which leads to an increase in the stored energy in them. In addition, because the voltage value of inductors is negative, their current is decreased. This state leads to a reduction in the stored energy in them. According to Fig. 2b and as the current value of the inductors $L_{1,1}$ and $L_{2,1}$ are equal to the current value of the inductors $L_{1,2}$ and $L_{2,2}$, it is concluded that the equations (1) to (3) are also verified in this operating mode. By applying KVL in Fig. 2b, it is inferred that:

$$2v_L + V_C = 0 \quad (8)$$

$$-V_i - V_C + 2v_L + v_{dc,\max} = 0 \quad (9)$$

By applying (8) and (9), we have:

$$v_{dc,\max} = 2V_C + V_i \quad (10)$$

In this operating mode, the output voltage is equal to the maximum dc link voltage value. Therefore, it is concluded that:

$$v_o = 2V_C + V_i \quad (11)$$

In addition, the voltage of diodes $D_{1,1}$, $D_{2,1}$, $D_{1,2}$ and $D_{2,2}$ is equal to:

$$v_{D1,1} = v_{D2,1} = v_{D1,2} = v_{D2,2} = v_L \quad (12)$$

By using (8) into (12), it is obtained that:

$$v_{D1,1} = v_{D2,1} = v_{D1,2} = v_{D2,2} = -0.5V_C \quad (13)$$

The equation (13) shows that the voltage of diodes $D_{1,1}$, $D_{2,1}$, $D_{1,2}$ and $D_{2,2}$ is negative and, thus, these diodes are turned off.

2.1.3. Third Operating Mode (Time Interval of $0.5(1+D_{ST})T_s \le t \le T_s$)

In the third operating mode, as shown in Fig. 2c, the switches of S_2 and S_3 are turned on and the switches of S_1 and S_4 are turned off; that leads to a negative output voltage level. In this operating mode, the voltage of the capacitors is increased; that leads to an increase in the stored energy in them. In addition, the inductors' current is decreased; that leads to a reduction in the stored energy in them. According to Fig. 2c and as the current value of the inductors $L_{1,1}$ and $L_{2,1}$ are equal to the current value of the inductors $L_{1,2}$ and $L_{2,2}$, it is concluded that the equations (1) to (3) are also verified in this operating mode. In addition, other obtained results as (8) to (10) are also verified in this mode because the circuit of this mode is the same as second operating mode except for its inverter side. The load voltage in this mode is calculated as follows:

$$v_o = -(2V_C + V_i) \quad (14)$$

It is pointed out that the voltage of diodes $D_{1,1}$, $D_{2,1}$, $D_{1,2}$ and $D_{2,2}$ in this operating mode is the same as the second operating mode.

Fig. 3 shows the voltage and current waveforms of the used devices in the proposed Z-source inverter. In this figure, all operating modes are completely specified. In addition, these figures reconfirm all the obtained theoretical analyses about different operating modes. It is important to note that G_{S1}, G_{S2}, G_{S3} and G_{S4} are the excitation voltage of the switches S_1, S_2, S_3 and S_4 respectively. In these figures, 1 means that the switch has turned on, and zero means that the switch has turned off. The control method of the proposed topology is based on the presented method in [24, 25].

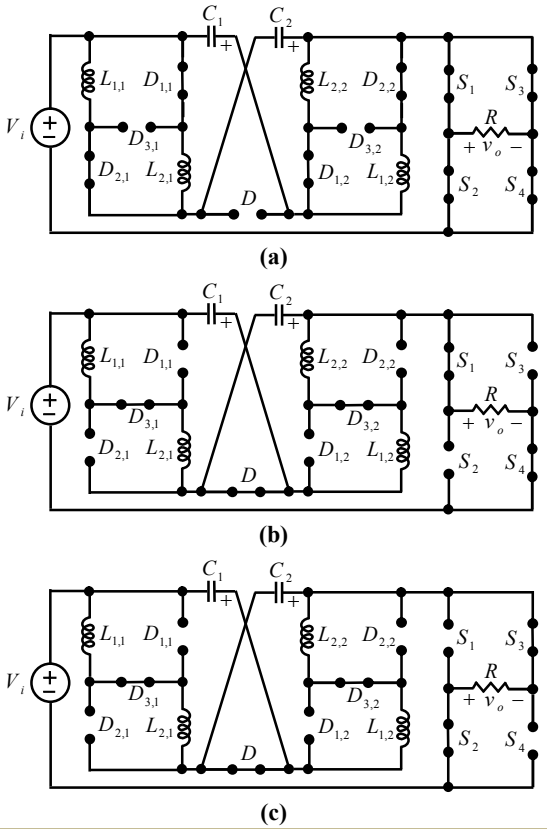


Fig. 2: The equivalent circuits of the proposed inverter in different operating modes. a) First operating mode. b) Second operating mode. c) Third operating mode

2.2. Voltage Gain Calculations

The voltage of the inductor is shown in Fig. 3. In order to calculate the voltage gain of the proposed inverter, the balance law of the inductor voltage is used. According to this law, the integral of the inductor voltage in a period is equal to zero. Therefore, we have:

$$\int_0^{T_s} v_L dt = 0 \qquad (15)$$

According to Fig. 3 and based on (15), it is concluded that:

$$\int_0^{0.5D_{ST}T_s} (V_C + V_i)dt - \int_{0.5D_{ST}T_s}^{0.5T_s} \frac{V_C}{2} dt = 0 \qquad (16)$$

By simplifying the (16), the average voltage value of the capacitors is calculated as follows:

$$V_C = \frac{2D_{ST}}{1-3D_{ST}} V_i \qquad (17)$$

By replacing (17) into (10), the maximum dc link voltage value is calculated as follows:

$$v_{dc,\max} = \frac{1+D_{ST}}{1-3D_{ST}} V_i = BV_i \qquad (18)$$

In (18), B is the boost factor (voltage gain).

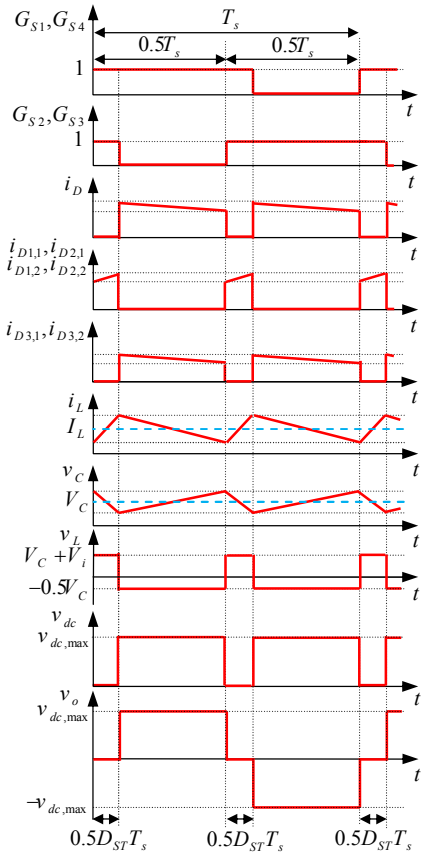


Fig. 3: The output voltage and current waveforms of the used devices in the proposed Z-source inverter

3. Proposed Developed Z-Source Inverter

If two switched inductor cells, each of which includes n numbers of inductors and $3n-3$ diodes, are used in the proposed inverter of Fig. 1, a new developed Z-source inverter is proposed. The developed Z-source inverter is shown in Fig. 4 and consists of a higher voltage gain. As it is shown in this figure, the proposed developed inverter includes inductors of $L_{1,1}$, $L_{2,1}$,… , $L_{n-1,1}$, $L_{n,1}$ and diodes of $D_{1,1}$, $D_{2,1}$, $D_{3,1}$, … , $D_{3n-5,1}$, $D_{3n-4,1}$ and $D_{3n-3,1}$ in the first cell and the inductors of $L_{1,2}$, $L_{2,2}$, … , $L_{n-1,2}$, $L_{n,2}$ and diodes of $D_{1,2}$, $D_{2,2}$, $D_{3,2}$, $D_{3n-5,2}$, $D_{3n-4,2}$ and $D_{3n-3,2}$ in the second cell. There are three operating modes in the developed proposed inverter the same as the proposed inverter in the previous section. The performance of the developed inverter in three-operating modes will be analyzed in the next sub-section.

3.1. Operating Modes of the Developed Proposed Inverter

The switching methods of the used power switches in the inverter and the turning on and off states of the diodes in the first cell, the second cell, and the diode of D determine the operating modes of the developed inverter.

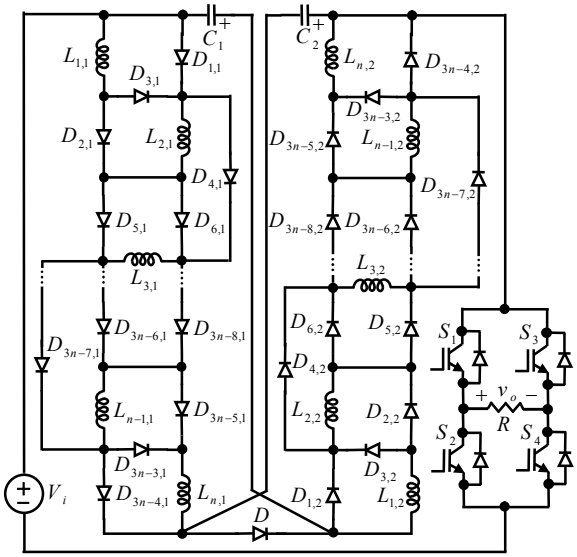


Fig. 4: Developed proposed Z-source inverter

3.1.1. The First Operating Mode (Time Interval of $0 \le t < 0.5D_{ST}T_s$)

This operating mode is shown in Fig. 5a. In this mode, all of the inverter's switches are turned on,

and the inverter is in ST state. In addition, the diodes of the cells are connected parallel to each other. In this operating mode, the voltages of all capacitors are decreased, and the inductor's currents are increased. Therefore, based on Fig. 5a, it is concluded that:

$$v_{L1,1} = v_{L2,1} = \cdots = v_{Ln,1} = v_L \quad (19)$$

$$v_{L1,2} = v_{L2,2} = \cdots = v_{Ln,2} = v_L \quad (20)$$

The equations of (4) to (6) in the first operating mode of the proposed inverter are also verified in this operating mode. In addition, the voltage of the diodes of $D_{3,1}$, $D_{6,1}$, …, $D_{3n-6,1}$ and $D_{3n-3,1}$ from the first cell and diodes of $D_{3,2}$, $D_{6,2}$, …, $D_{3n-6,2}$ and $D_{3n-3,2}$ from the second cell that are turned off and have negative values calculated as follows:

$$v_{D3,1} = v_{D6,1} = \cdots = v_{D3n-6,1} = v_{D3n-3,1} = -V_C - V_i \quad (21)$$

$$v_{D3,2} = v_{D6,2} = \cdots = v_{D3n-6,2} = v_{D3n-3,2} = -V_C - V_i \quad (22)$$

The performance of the proposed inverter in the time interval of $0.5T_s \le t < 0.5(1+D_{ST})T_s$ is the same as this mode.

3.1.2. The Second Operating Mode (Time Interval of $0.5D_{ST}T_s \le t < 0.5T_s$)

In the second operating mode, as shown in Fig. 5b, the switches of S_1 and S_4 are turned on, and the switches of S_2 and S_3 are turned off. Therefore, the positive voltage levels are generated at the output, and the inductors of the cells are connected in series. In this operating mode, the stored energy in capacitors is increased, and the stored energy in the inductors is decreased. According to Fig. 5b, as the current value of the inductors of $L_{1,1}$, $L_{2,1}$, … and $L_{n,1}$ from the first cell are equal to the current value of the inductors of $L_{1,2}$, $L_{2,2}$, … and $L_{n,2}$ from the second cell, it is concluded that the equations (19) and (20) are also verified in this operating mode. By applying KVL in Fig. 5b, it is concluded that:

$$nv_L + V_C = 0 \quad (23)$$

$$-V_i - V_C + nv_L + v_{dc,\max} = 0 \quad (24)$$

By applying (23) and Fig. 5b, the voltages of the diodes $D_{1,1}$, $D_{4,1}$, …, $D_{3n-8,1}$ and $D_{3n-5,1}$ from the first cell and the diodes of $D_{1,2}$, $D_{4,2}$, …, $D_{3n-8,2}$ and $D_{3n-5,2}$ from the second cell are calculated as follows:

$$v_{D1,1} = v_{D4,1} = \cdots = v_{D3n-8,1} = v_{D3n-5,1} = -\frac{V_C}{n} \quad (25)$$

$$v_{D1,2} = v_{D4,2} = \cdots = v_{D3n-8,2} = v_{D3n-5,2} = -\frac{V_C}{n} \quad (26)$$

In addition, the voltages of the turned-off diodes of $D_{2,1}$, $D_{5,1}$, …, $D_{3n-7,1}$ and $D_{3n-4,1}$ from the first cell and of the turned-off diodes of $D_{2,2}$, $D_{5,2}$, …, $D_{3n-7,2}$ and $D_{3n-4,2}$ from the second cell are calculated as follows:

$$v_{D2,1} = v_{D5,1} = \cdots = v_{D3n-7,1} = v_{D3n-4,1} = -\frac{V_C}{n} \quad (27)$$

$$v_{D2,2} = v_{D5,2} = \cdots = v_{D3n-7,2} = v_{D3n-4,2} = -\frac{V_C}{n} \quad (28)$$

By using (23), (24), and based on Fig. 5b, the load voltage that is equal to maximum dc link voltage is calculated as follows:

$$v_o = v_{dc,\max} = 2V_C + V_i \quad (29)$$

3.1.3. The Third Operating Mode (Time Interval of $0.5(1+D_{ST})T_s \le t \le T_s$)

In the third operating mode, as shown in Fig. 5c, the switches of S_2 and S_3 are turned on, and the switches of S_1 and S_4 are turned off. Therefore, negative voltage levels are generated at the output, and the inductors of the cells are connected in series. In this operating mode, the voltage of the capacitors is increased, and the inductors' current is decreased. According to Fig. 5c and as the current value of the inductors $L_{1,1}$, $L_{2,1}$, … and $L_{n,1}$ from the first cell are equal to the current value of the inductors $L_{1,2}$, $L_{2,2}$, … and $L_{n,2}$ from the second cell, it is concluded that the equations (19) and (20) are also verified in this operating mode. In addition, other obtained results from (23) to (28) are also verified in this mode because the circuit of this mode is the same as the second operating mode except for its inverter side. The load voltage in this mode is calculated as follows:

$$v_o = -(2V_C + V_i) \quad (30)$$

It is pointed out that the voltage of the turned off diodes in this operating mode is the same as the second operating mode.

3.2. Voltage Gain Calculations

The voltage gain of the developed inverter is calculated by applying (4) and (23) into (15) as

follows:

$$\int_0^{0.5D_{ST}T_s}(V_C+V_i)dt-\int_{0.5D_{ST}T_s}^{0.5T_s}\frac{V_C}{n}dt=0 \quad (31)$$

By simplifying the (31), the voltage of the capacitor is calculated as follows:

$$V_C=\frac{nD_{ST}}{1-(n+1)D_{ST}}V_i \quad (32)$$

By replacing (32) into (24), the maximum value dc link voltage is calculated as follows:

$$v_{dc,\max}=\frac{1+(n-1)D_{ST}}{1-(n+1)D_{ST}}V_i=BV_i \quad (33)$$

4. Capacitor's Voltage Ripple and Inductor's Current Ripple Calculations

Two main parameters in the Z-source inverters are the capacitor's voltage ripple and the inductor's current ripple. Therefore, achieving a suitable design of the capacitor and inductor in the proposed inverter necessitates the calculation ation of the capacitor's voltage ripple and inductor's current ripple [26].

4.1. Inductor's Current Ripple Calculation

In the proposed inverter, the calculation of the inductors' current ripple (Δi_L) requires the use of the equation $v_L=L\frac{di_L}{dt}$ and (8). Therefore, we have:

$$-0.5V_C=L\frac{2\Delta i_L}{(1-D_{ST})T_s} \quad (34)$$

By replacing (17) into (34), the value of Δi_L is calculated as follows:

$$|\Delta i_L|=\frac{D_{ST}(D_{ST}-1)T_s}{2L(1-3D_{ST})}V_i \quad (35)$$

In order to calculate the inductors' current ripple in the developed inverter, the equations (23) and (32) are used as follows:

$$|\Delta i_L|=\frac{D_{ST}(D_{ST}-1)T_s}{2L[1-(n+1)D_{ST}]}V_i \quad (36)$$

As it is clear, the (35) is the specific state of the (36) when $n=2$.

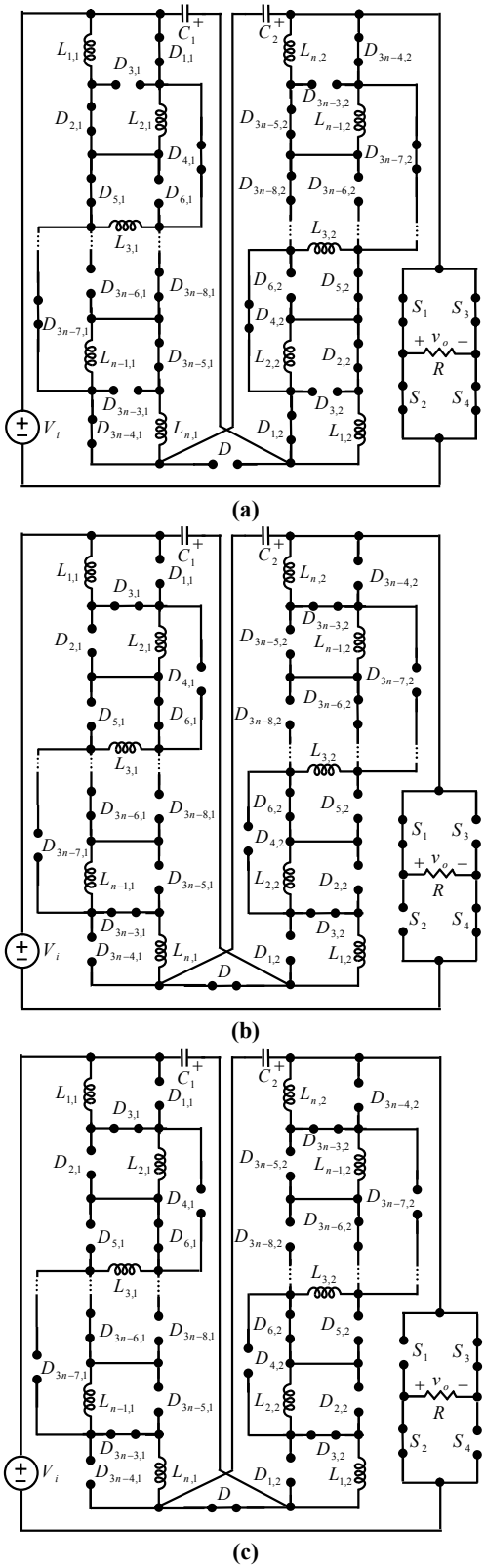


Fig. 5: The equivalent circuits of the developed proposed inverter in different operating modes. a) The first operating mode. b) The second operating mode. c) The third operating mode

4.2. Capacitor's Voltage Ripple Calculation

As it is shown in Fig. 2a, the current of the capacitors and inductors of the proposed inverter in ST state is obtained as follows:

$$2i_L = -i_C \tag{37}$$

By using the equation $i_C = C\frac{dv_C}{dt}$, the equation of (37) is rewritten as follows:

$$|\Delta v_C| = \frac{D_{ST}T_s}{C} I_L \tag{38}$$

In (38), I_L is the average value of the inductor's current and $|\Delta v_C|$ is the capacitor's voltage ripple.

As shown in Fig. 5a the current of the capacitors and inductors of the developed proposed inverter in ST state is obtained as follows:

$$ni_L = -i_C \tag{39}$$

By using (39), the capacitors' voltage ripple in the developed proposed inverter is calculated as follows:

$$|\Delta v_C| = \frac{nD_{ST}T_s}{2C} I_L \tag{40}$$

As it is clear, the equation (38) is the specific state of (40) when $n = 2$.

In addition, it is obvious from (38) and (40) that the average value of the inductor's current has effects on the value of the capacitor's voltage ripple in such a way that by increasing the value of the inductor's current, the capacitor's voltage ripple is increased. Also, by reducing the value of the inductor's current, the capacitor's voltage ripple is decreased. Therefore, it is necessary to calculate the average value of the inductor's current. In order to calculate the average value of the inductor's current, the integral of the capacitor's current, that is equal to zero in a period, is used. Therefore, we have:

$$\int_0^{T_s} i_C dt = 0 \tag{41}$$

By applying (18) and (37) and by using KCL in the circuit of Fig. 2b, the equation (41) is rewritten as follows:

$$\int_0^{0.5D_{ST}T_s} (-2I_L)dt + \int_{0.5D_{ST}T_s}^{0.5T_s} \left[I_L - \frac{1+D_{ST}}{R(1-3D_{ST})} V_i \right] dt = 0 \tag{42}$$

In (42), R is the load resistance.

By simplifying the (42), the value of I_L is calculated as follows:

$$I_L = \frac{(1-D_{ST})(1+D_{ST})}{R(1-3D_{ST})^2} V_i \tag{43}$$

In order to calculate the value of I_L in the developed proposed inverter, the equations of (33) and (39) and the KCL in Fig. 5b are used, which are equal to:

$$\int_0^{0.5D_{ST}T_s} (-nI_L)dt + \int_{0.5D_{ST}T_s}^{0.5T_s} \left[I_L - \frac{1+(n-1)D_{ST}}{R[1-(n+1)D_{ST}]} V_i \right] dt = 0 \tag{44}$$

By simplifying the (44), the average value of the inductors' current is calculated as follows:

$$I_L = \frac{(1-D_{ST})[1+(n-1)D_{ST}]}{R[1-(n+1)D_{ST}]^2} V_i \tag{45}$$

As it is obvious, the equation (43) is a specific state of equation (45). Equation (45) shows that by reducing the value of the output load, the value of the current through inductors is increased. This issue can be resulted in the saturation of inductors. To prevent this occurrence, there are, also, other methods to construct variable inductors using powdered metal core, but it is not related to the objectives of this paper [27].

5. Comparison of the Proposed Topology with the Conventional Z-source Inverters

The main aim of the proposed topology is increasing the voltage gain and decreasing the voltage stress of the capacitors. In this section, in order to investigate the advantages and disadvantages of the proposed inverter, we compared this topology with those conventional Z-source inverters which have been presented in [1], [14-16], [21-22], and [26]. A higher voltage gain becomes possible by increasing the time interval of the ST state and the number of inductors in the switched inductor cells, Fig. 6 shows the comparison of the voltage gain in the proposed inverter with the conventional Z-source inverters versus D_{ST}. For instance, the voltage gain of the conventional Z-source inverter is equal to 1.43 by considering $D_{ST} = 0.15$, while the voltage gain of the proposed inverter is equal to 2.09 by considering $n = 2$ in the same condition. However, this value is increased to 3.25 when $n = 3$ and is increased to 5.8 when $n = 4$. It is noticeable that the boost factor of proposed topology is equal to the boost factor of the presented topology in [26].

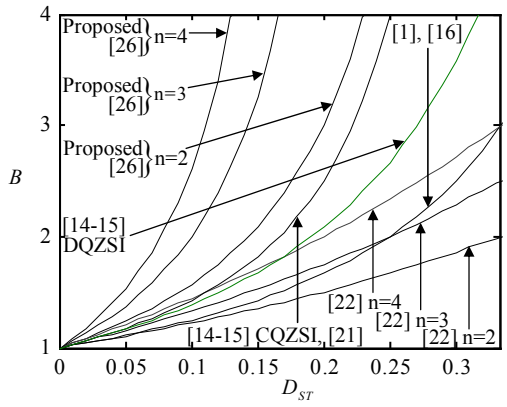


Fig. 6: The comparison of the voltage gain in the proposed inverter

Fig. 7 shows the comparison of the maximum voltage stress of the capacitors in the proposed inverter and the conventional Z-source inverters. The maximum voltage stress is considered in this comparison because the voltage stress of the capacitors differ in different topologies, and that is shown by $V_{C,\max}$. As it is obvious from this figure, the maximum value of the capacitors' voltage stress in the proposed inverter is lower than other conventional Z-source inverters, while the minimum value of D_{ST} is considered. This leads to several advantages such as decreasing the cost of the inverter because of decreasing the nominal value of the capacitors. In addition, the voltage stress value of the capacitors is equal to zero when D_{ST} is equal to zero. Therefore, it is possible to increase the value of the voltage stress of the capacitors by controlling the value of D_{ST} from zero to the desired value, which results in a soft start. It is important to note that it is impossible to use a soft start in the conventional Z-source inverters that are considered in this comparison. It is noticeable that maximum value of dc-link voltage in [26] is equal to the average value of voltage across the capacitor. Hence, in high voltage gain, voltage stress on the capacitor is extremely increased. Another advantage of the proposed inverter is the existence of the common ground between the input source and the stage of the inverter, whereas the presented topologies in [21] and [26] do not have a common ground. The lack of common ground between the input source and the stage of the inverter is resulted in the limitation of applying the topology in renewable energy systems. Table I shows the comparison of the voltage gain and the voltage stress of the capacitors in the proposed inverter with the conventional Z-source inverters.

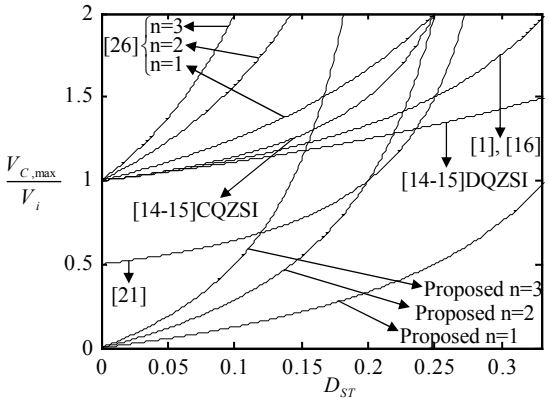


Fig. 7: The comparison of the maximum voltage stress of the capacitors in the proposed inverter and the conventional Z-source inverters

6. Simulation Results

In order to verify the accuracy performance of the proposed inverter, the simulation results on the proposed inverter by considering $n=2$ in EMTDC/PSCAD software programs are used. Table II shows the selected values of the devices and other parameters in simulation.

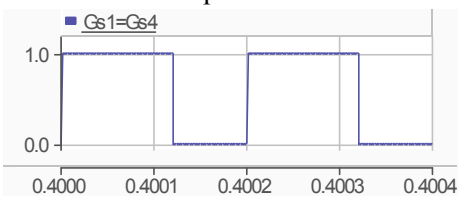
Table 1: The comparison of the voltage gain and voltage stress of the capacitors

	B	$\frac{V_{C1}}{V_i}$	$\frac{V_{C2}}{V_i}$	$\frac{V_{C3}}{V_i}$
ZSI [1]	$\frac{1}{1-2D_{ST}}$	$\frac{1-D_{ST}}{1-2D_{ST}}$	$\frac{1-D_{ST}}{1-2D_{ST}}$	-
L-ZSI [22]	$\frac{1+(n-1)D_{ST}}{1-D_{ST}}$	-	-	-
CQZSI [14-15]	$\frac{1}{1-3D_{ST}}$	$\frac{D_{ST}}{1-3D_{ST}}$	$\frac{D_{ST}}{1-3D_{ST}}=\frac{V_{C4}}{V_i}$	$\frac{1-2D_{ST}}{1-3D_{ST}}$
DQZSI [14-15]	$\frac{1}{(1-D_{ST})(1-2D_{ST})}$	$\frac{D_{ST}}{(1-D_{ST})(1-2D_{ST})}$	$\frac{D_{ST}}{(1-D_{ST})(1-2D_{ST})}$	$\frac{1}{1-D_{ST}}$
Cascaded-ZSI [21]	$\frac{1}{1-3D_{ST}}$	$\frac{1-D_{ST}}{2(1-3D_{ST})}$	$\frac{1-D_{ST}}{2(1-3D_{ST})}$	-
QZSI [13]	$\frac{1}{1-2D_{ST}}$	$\frac{1-D_{ST}}{1-2D_{ST}}$	$\frac{D_{ST}}{1-2D_{ST}}$	-
Switched-ZSI [26]	$\frac{1+(n-1)D_{ST}}{1-(n+1)D_{ST}}$	$\frac{1+(n-1)D_{ST}}{1-(n+1)D_{ST}}$	-	-
Proposed	$\frac{1+(n-1)D_{ST}}{1-(n+1)D_{ST}}$	$\frac{nD_{ST}}{1-(n+1)D_{ST}}$	$\frac{nD_{ST}}{1-(n+1)D_{ST}}$	-

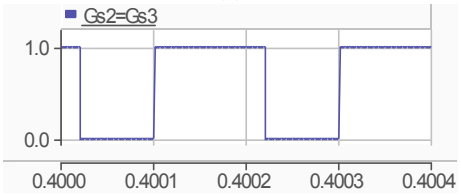
Table 2: The Selected values in simulation

V_i	20V
$L_{1,1} = L_{1,2} = L_{2,1} = L_{2,2}$	5mH
$C_1 = C_2$	680μF
$r_{switch-on}$	0.01Ω
$r_{switch-off}$	$10^6\Omega$
$r_{diode-on}$	0.01Ω
$r_{diode-off}$	$10^6\Omega$
R	25Ω
f_s	5kHz

Fig. 8 shows the simulation results of the proposed inverter. Figs. 8a and 8b show the applied pulses to the power switches, which leads to ST state by using $D_{ST} = 0.2$. Fig. 8c shows the current of the diode. This figure reconfirms that the diode is turned off in ST state. Fig. 8d shows the current of diodes $D_{3,1}$ and $D_{3,2}$ that are turned off in ST state, and their current is the same as inductors' current in non-ST states. Fig. 8e shows the current of diodes $D_{1,1}$, $D_{1,2}$, $D_{2,1}$, and $D_{2,2}$ that are turned on in ST state, and their current is the same as inductors' current. In non-ST states, they are turned off, and, as a result, their current is equal to zero. Fig. 8f shows the current of the inductors. As it illustrated in this figure, the current ripple of these inductors are equal to 0.15 A, which is very close to the obtained value from (35) and is equal to 0.16 A. In addition, the average value of the inductors' current is equal to 4.72 A, which is very close to the obtained value by (43) and is equal to 4.8 A. Fig. 8g shows the voltage of the inductor. As it is shown in this figure, the voltage of the inductors in ST state is positive and equal to 39.26V, while in non-ST state this value is equal to 9.82V. It is important to note that these values are very close to the obtained values from (4) and (8) which are equal to 40V and 10V respectively. Fig. 8h shows the voltage of the capacitors. According to this figure, the voltage ripple of the capacitors is equal to 0.279V, and the average value of capacitors' voltage is equal to 19.53V, while these values by (17) and (38) are 0.28V and 20V respectively. Figs. 8i and 8j show the capacitor's current and dc link voltage, respectively. These figures completely verify the theoretical issues in the previous sections. Finally, Fig. 8k shows the output voltage of the inverter that includes three levels: positive, negative, and zero levels. In addition, the value of the positive level is equal to 59.075V, which is very close to the obtained result from theoretical equation as 60V.



(a)



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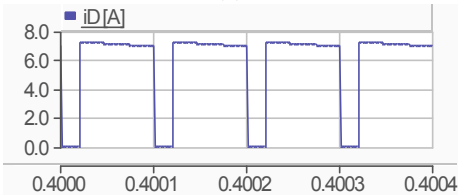
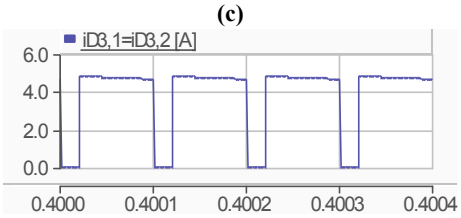
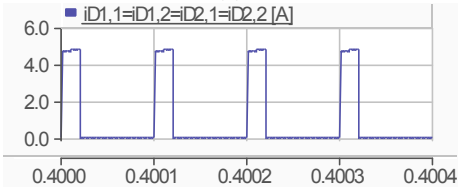


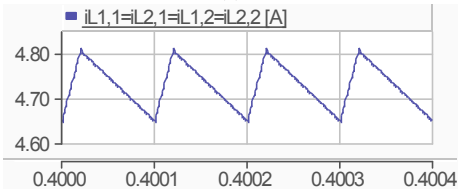
(c)



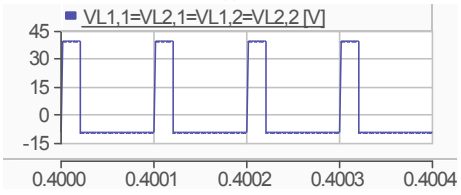
(d)



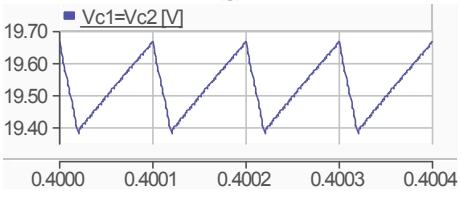
(e)



(f)



(g)



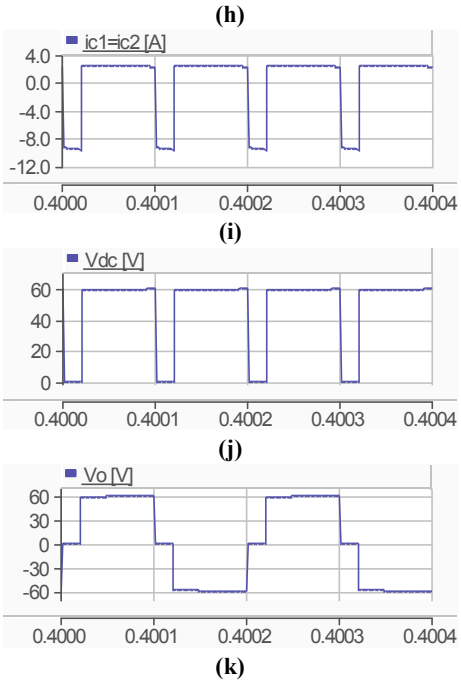


Fig. 8: Simulation results of the proposed inverter with $D_{ST} = 0.2$. a) Applied pulses to the power switches of S_1 and S_4. b) Applied pulses to the power switches of S_2 and S_3. c) Current of the diode D. d) Current of the diodes $D_{3,1}$ and $D_{3,2}$. e) Current of the diodes $D_{1,1}$, $D_{1,2}$, $D_{2,1}$ and $D_{2,2}$. f) Current of the inductors $L_{1,1}$, $L_{1,2}$, $L_{2,1}$ and $L_{2,2}$. g) Voltage of the inductors $L_{1,1}$, $L_{1,2}$, $L_{2,1}$ and $L_{2,2}$. h) Voltage of the capacitors C_1 and C_2. i) Current of the capacitors. j) DC-link voltage. k) Output voltage.

7. Conclusion

In this paper, a new series Z-source inverter topology based on switched inductor cells is proposed. In this topology, different operating modes are investigated and the voltage gain is calculated based on $n \geq 2$. In addition, the calculated voltage gain in the proposed inverter is compared with the conventional Z-source inverters. According to this comparison, the proposed inverter is able to increase the voltage gain. Moreover, in the proposed inverter, the capacitors' voltage stress is calculated. This value in the proposed inverter is also lower than the conventional Z-source inverters. For instance, the voltage gain of the proposed inverter by considering $n = 2$ and $D_{ST} = 0.25$ is equal to 5; that is, 2.5 of the voltage gain in the conventional Z-source inverter with the same value of D_{ST}. Following, the capacitors' voltage ripple, the inductors' current ripple and the average current values of inductors are also calculated. The accuracy performance of the proposed inverter is verified through simulation results in EMTDC/PSCAD software programs.

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